

# ISITEP

## D4.2.3 - E1 ISI TETRA GATEWAY PROTOTYPE FOR DEMONSTRATIONS, FINAL RELEASE

<b>Document Manager:</b>	Kirsten Aabye	MOT	Editor
--------------------------	---------------	-----	--------

<b>Programme:</b>	Inter System Interoperability for Tetra-TetraPol Networks
<b>Project Acronym:</b>	ISITEP
<b>Contract Number:</b>	312484
<b>Project Coordinator:</b>	Selex ES
<b>SP Leader:</b>	Jaakko Saijonmaa (ADSFI)

<b>Document ID N°:</b>	E1_ISI_GW_D4.2.3_17052016	<b>Version:</b>	V1.0
<b>Deliverable:</b>	D4.2.3	<b>Date:</b>	17/05/2016
		<b>Status:</b>	Final

<b>Document classification</b>	<b>Public</b>
--------------------------------	---------------

Approval Status	
<b>Prepared by :</b>	Kirsten Aabye (MOT)
<b>Approved by (WP Leader) :</b>	Christian Bjerrum-Niese (MOT)
<b>Approved by (SP Leader) :</b>	Jaakko Saijonmaa (ADSFI)
<b>Approved by (Coordinator)</b>	<b>To Approve</b> Paolo Di Michele (SES)

**Security Approval  
(Advisory Board Coordinator)**

**To Approve** Etienne Lezaack (BFP)

## CONTRIBUTING PARTNERS

Name	Company / Organization	Role / Title
Kirsten Aabye	Motorola Solutions	Contributor/Editor

## DISTRIBUTION LIST

Name	Company / Organization	Role / Title
Kirsten Aabye	MOT	Editor
Christian Bjerrum-Niese	MOT	4.2 Leader
Jaakko Saijonmaa	CAS FI	SP leader
Liisa Laaksonen	CAS FI	4.2 Participant
Janne Nohkola	CAS FI	4.2 Participant
Timo Toikkanen	CAS FI	4.2 Participant
Marianne Storrøsten	DNK	4.2 Participant
Michel Duits	DNK	4.2 Participant
Anita Galin	MSB	4.2 Participant
Fredrik Lind	MSB	4.2 Participant
Robert Danelius	MSB	4.2 Participant

## REVISION TABLE

Version	Date	Modified Pages	Modified Sections	Comments
V0.1	03/05/2016	All	All	First draft
V1.0	17/05/2016	-	Header numbering	Final

### **Publishable extended abstract**

This Document is describing the completion of Task 4.2.2 “Interface design” and Task 4.2.3 “Gateway design and development”

The objective of the E1 ISI TETRA gateway interface is to allow TETRA networks, that provide current TETRA ISI standard interface (E1/QSIG/ROSE based) to be interconnected to TETRA networks, that provide an IP based ISI, as being defined in ISITEP WP4.1. The upper layers of the ETSI ISI standard remain unchanged and their interoperability is handled in ISITEP WP4.7, beyond the scope of this delivery.



## CONTENTS

<b>1. INTRODUCTION .....</b>	<b>6</b>
<b>1.1 Introduction .....</b>	<b>6</b>
<b>2. DESCRIPTION .....</b>	<b>7</b>
<b>2.1 Requirement Fulfillment .....</b>	<b>7</b>
<b>2.2 Software Development.....</b>	<b>7</b>
<b>2.3 HW Selection .....</b>	<b>8</b>
<b>2.4 Testing and Validation .....</b>	<b>9</b>
<b>3. REFERENCES .....</b>	<b>10</b>

## 1. INTRODUCTION

### 1.1 Introduction

One of the goals for the ISITEP program is to define how Inter System Interface (ISI) signalling between TETRA SwMIs can be conveyed in an SIP/IP network. The current ISI specifications describe how ISI signalling is conveyed in a QSIG/E1 network where the ISI signalling is included in Facility information elements. In order for the systems complying to the current standard to interconnect with the systems complying with the future standard a converter is to be introduced.

In task 4.1.1 a definition of ISI over IP was performed. In this protocol definition the ETSI ISI QSIG ROSE / E1 layer will be translated into SIP / IP protocol suite

One of the requirements towards the ISITEP program is that the ISI messages shall be unchanged and independent on the transport media.

As a result of task 4.2.1 a requirement specification for the E1 ISI TETRA gateway was developed.

Task 4.2.2 “Interface Design” has result in the development of the code for the E1 ISI TETRA gateway

Task 4.2.3 “Gateway Design and Development” has result in the deployment of the E1 ISI TETRA gateway on appropriate hardware.

The result of task 4.2.2 and 4.2.3 is a prototype which is ready for the demonstrations.

Task 4.2.4 “Testing and Validation” has been performed in connection to the test of the Motorola ISI over IP gateway.

## 2. DESCRIPTION

### 2.1 Requirement Fulfillment

The software has been created according to the requirements specified in D4.2.1 “E1 ISI TETRA gateway interface design documentation”. Since the requirements have been specified draft ETSI standard documents have been issued.

The E1 ISI TETRA gateway supports the following ETSI standards on the E1 side:

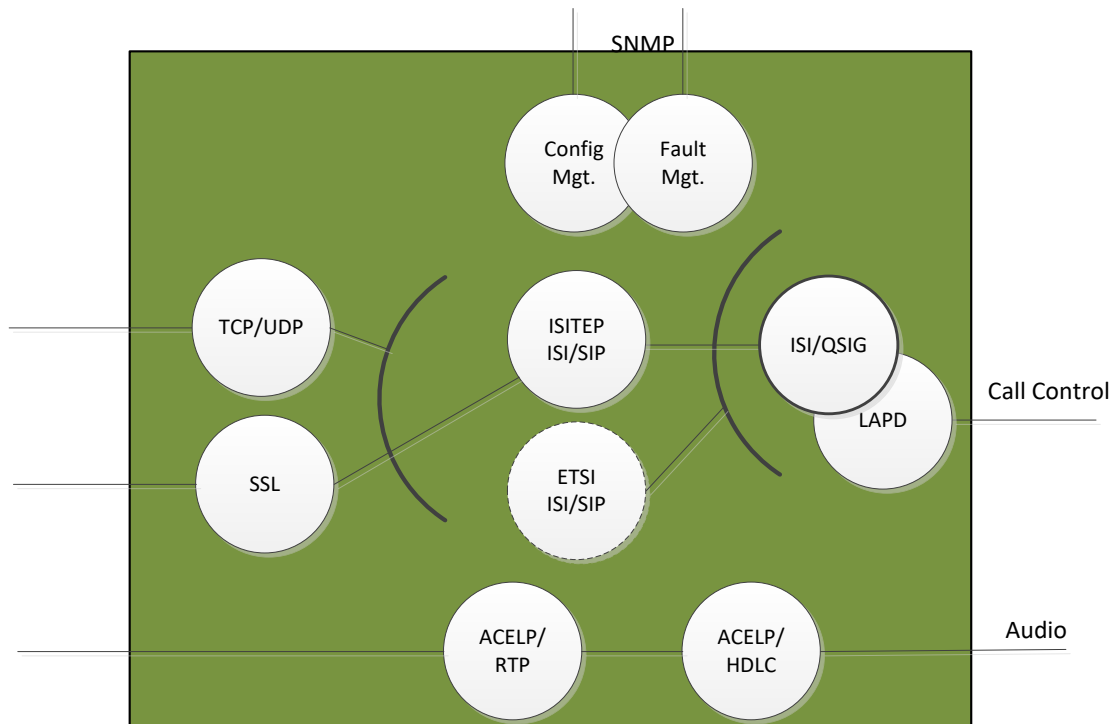
- TS 100 392-3-8  
"Generic Speech Format Implementation";
- TS 100 392-3-9  
"Transport Layer Independent Specification General design, Common Part";
- TS 100 392-3-10:  
"General design, PSS1/E.1 as transport layer ";

The E1 ISI TETRA gateway supports the following ETSI standards on the IP side:

- TS 100 392-3-8  
"Generic Speech Format Implementation";
- TS 100 392-3-9  
"Transport Layer Independent Specification General design, Common Part";
- TS 100 392-3-11  
"General design, SIP/IP as transport layer ";

### 2.2 Software Development

The software has been created according to the requirements specified in D4.2.1 “E1 ISI TETRA gateway interface design documentation”.



**Figure 1 E1 ISI TETRA Gateway Architecture**

The prototype software is developed in modules, which makes it possible to replace protocol layers with new version as the ISI over IP protocol evolves.

## 2.3 HW Selection

The required HW for the E1 ISI TETRA gateway shall be able to handle 4 E.1 links which comprises 120 sustained calls. Both call control and audio conversion (RTP to HDLC) are handled by the same server. This means that the processor shall be able to locally route 120 sustained calls without introducing an additional delay or jitter. The following requirements are located

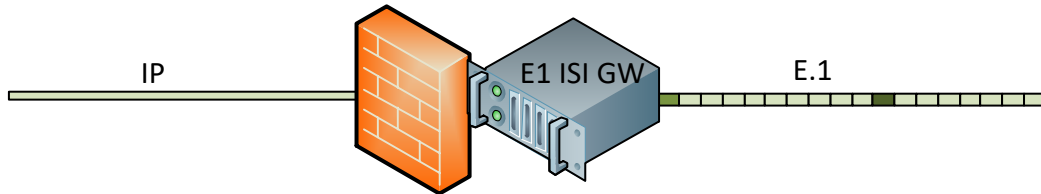
- Minimum 2 Gbit RAM
- Minimum 10 Gbit HDD
- Minimum 1.8 GHz CPU preferable with 8 cores
- 1 PCI slot (for the E.1 card)
- Minimum 2 VLAN ports
- Redundant power supply
- Rack mountable

Based on the above mentioned HW requirements Motorola has selected HP ProLiant DL360 Gen9 for the prototype of the E1 ISI TETRA gateway.

The E.1 card used in the E1 ISI TETRA gateway is PCE385 from Sunhillo

The firewall selected for the E1 ISI TETRA gateway communication across the IP network is selected based in the requirements listed in D4.6.2. The Fortigate FG firewall 100D from Fortinet is selected.





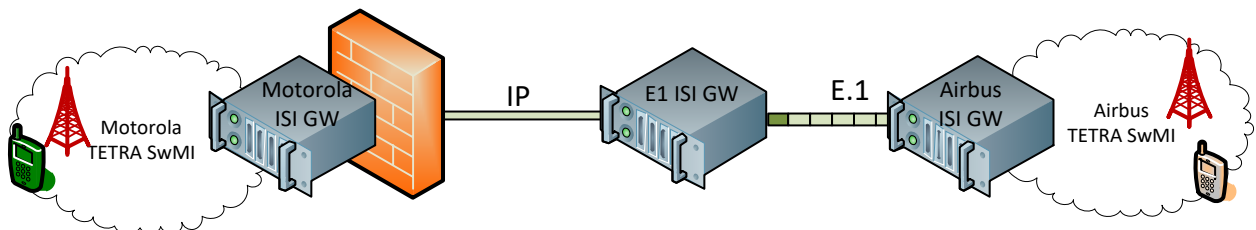
**Figure 2 E1 ISI TETRA Gateway Deployment**

## 2.4 Testing and Validation

The software has been deployed on a HP ProLiant DL360 Gen9 server.

The E1 ISI TETRA Gateway has been tested in the following environment:

- Internally as part of the factory test as described in D4.7.2 “Factory Test Report on Gateway and Network Elements Integration”.
- In relation to interconnection of the ISI over IP Gateway connected to the Airbus ISI Gateway



**Figure 3 E1 ISI TETRA Gateway Interconnection**

### 3. REFERENCES

- [1] D4.2.1 "E1 ISI TETRA gateway interface design documentation"
- [2] TS 100 392-3-8 V1.3.1  
"Generic Speech Format Implementation"
- [3] TS 100 392-3-9 V0.0.3  
"Transport Layer Independent Specification General design, Common Part"
- [4] TS 100 392-3-10:  
"General design, PSS1/E.1 as transport layer "
- [5] TS 100 392-3-11 V0.0.3  
"General design, SIP/IP as transport layer "